



Scaling Software Security Analysis to Satellites

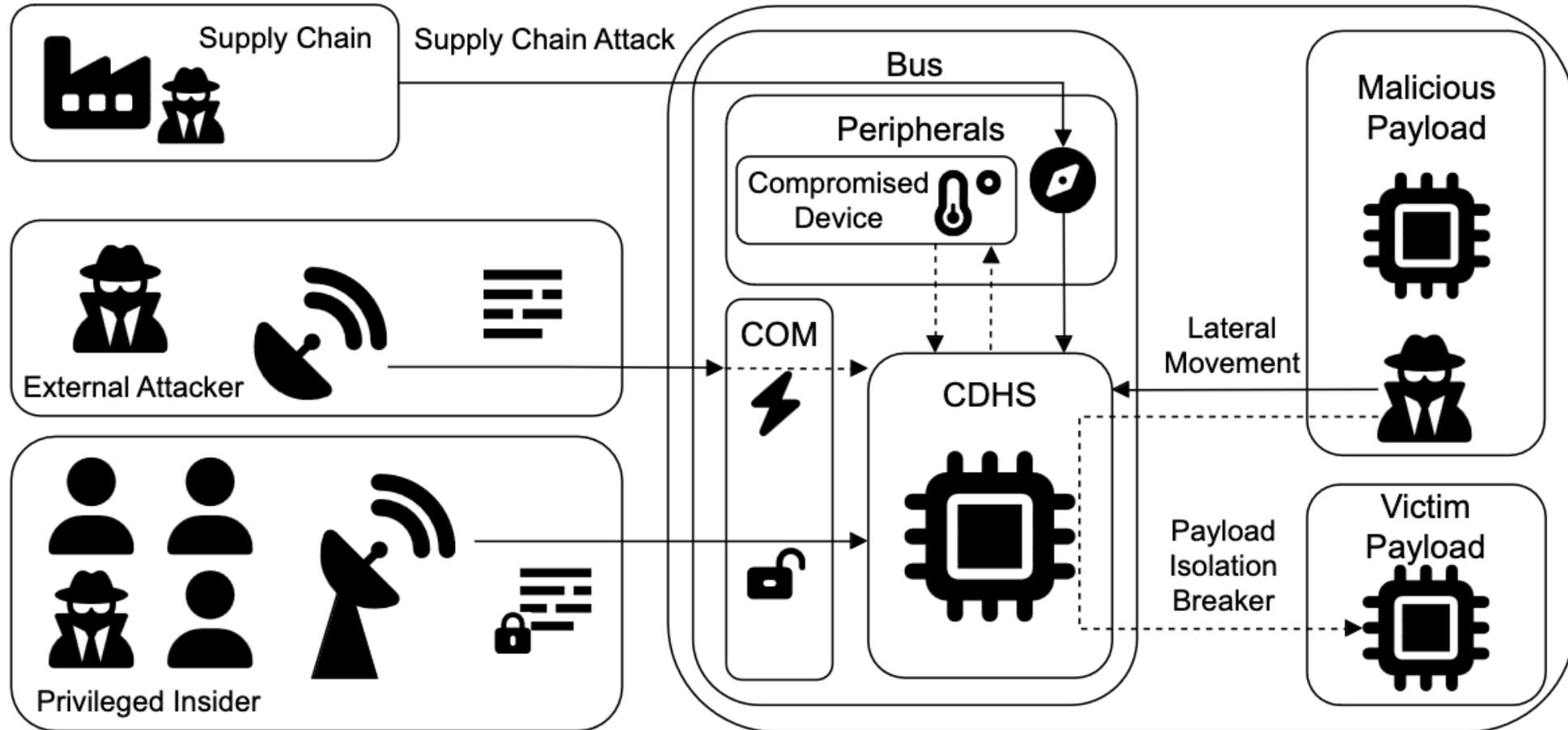
Automated Fuzz Testing and Its Unique Challenges

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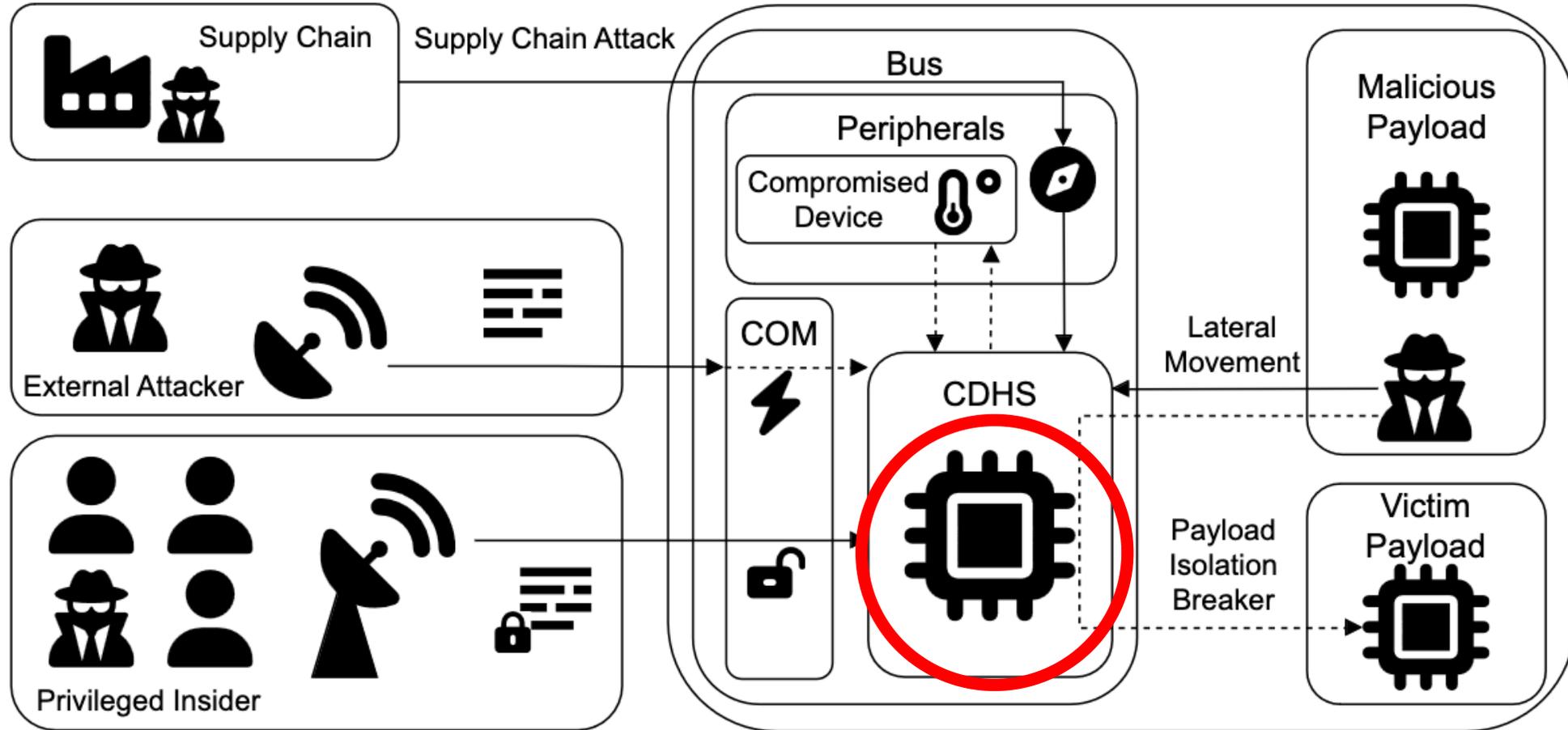
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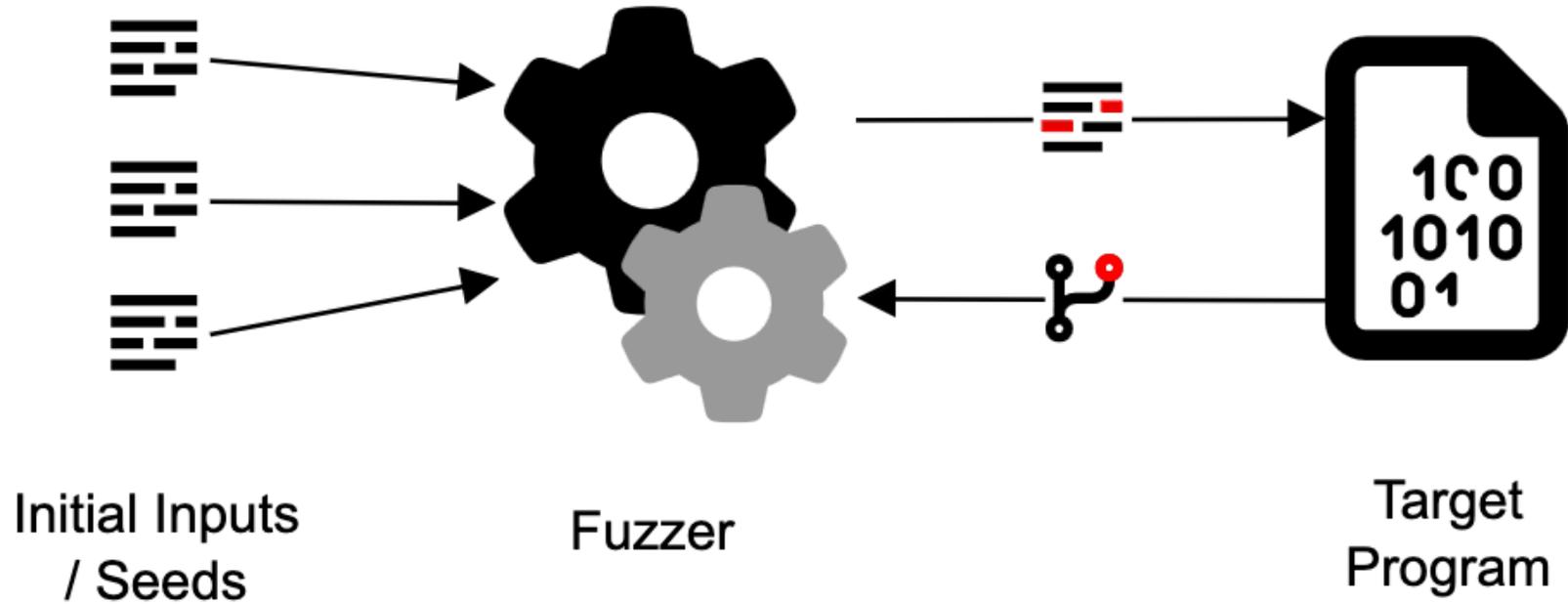
Scenario



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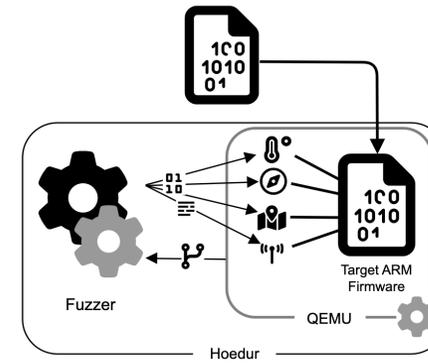
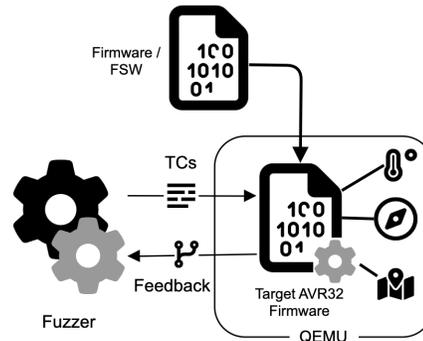
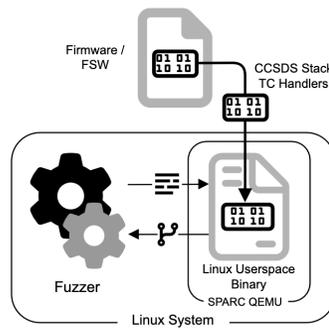
Fuzzing



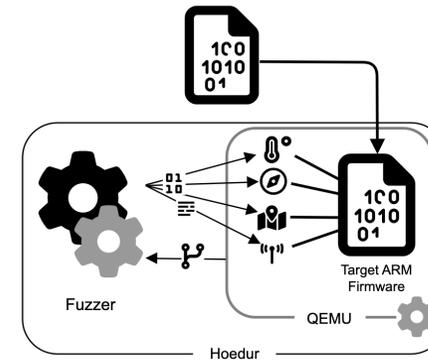
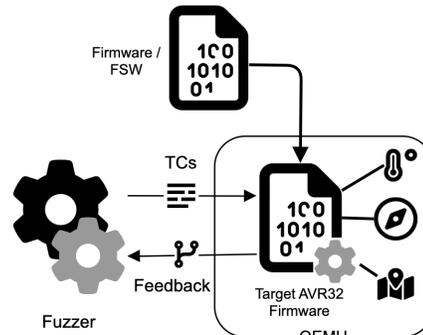
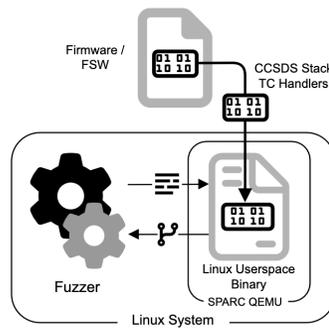
Challenges

1. Complex Satellite Boot Process
2. Only Crashing Inputs
3. Computing Hardware with Limited-Performance
4. Highly Specialized and Individual Setups
5. Performance of Existing Digital Twins

Approaches

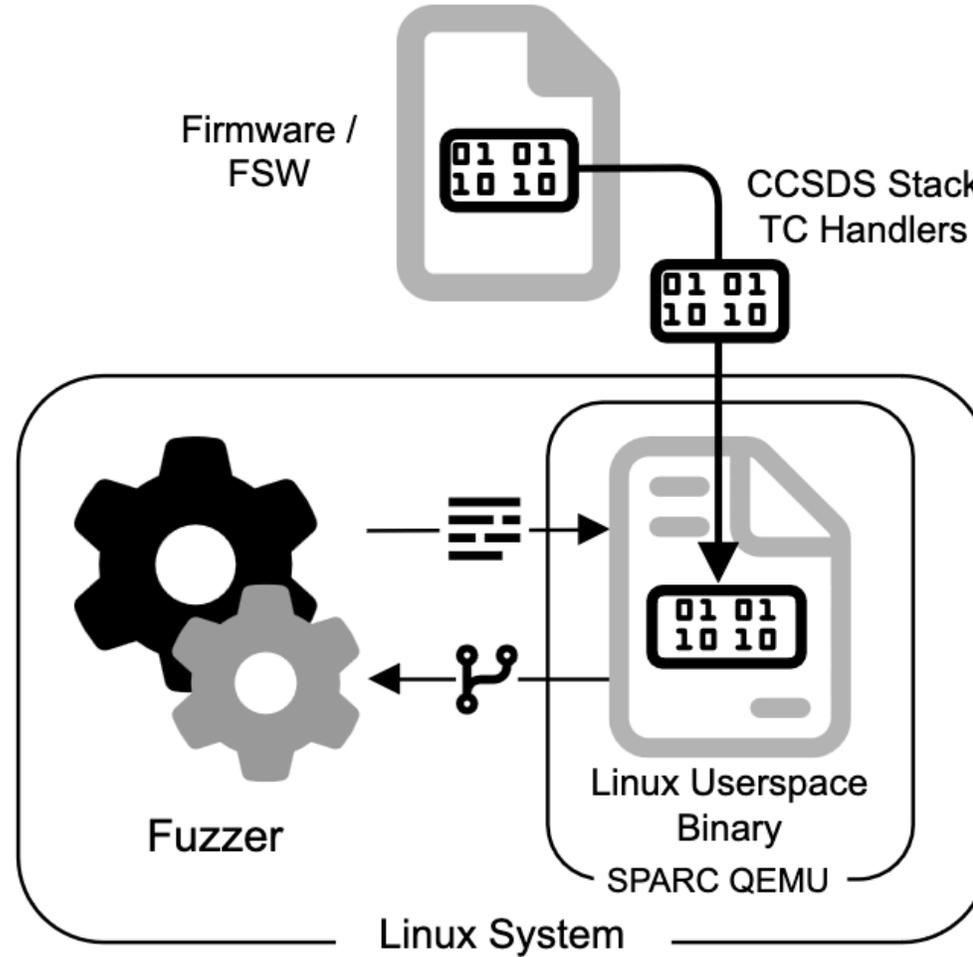


Approaches



=> No Hardware

Subsystem Extraction

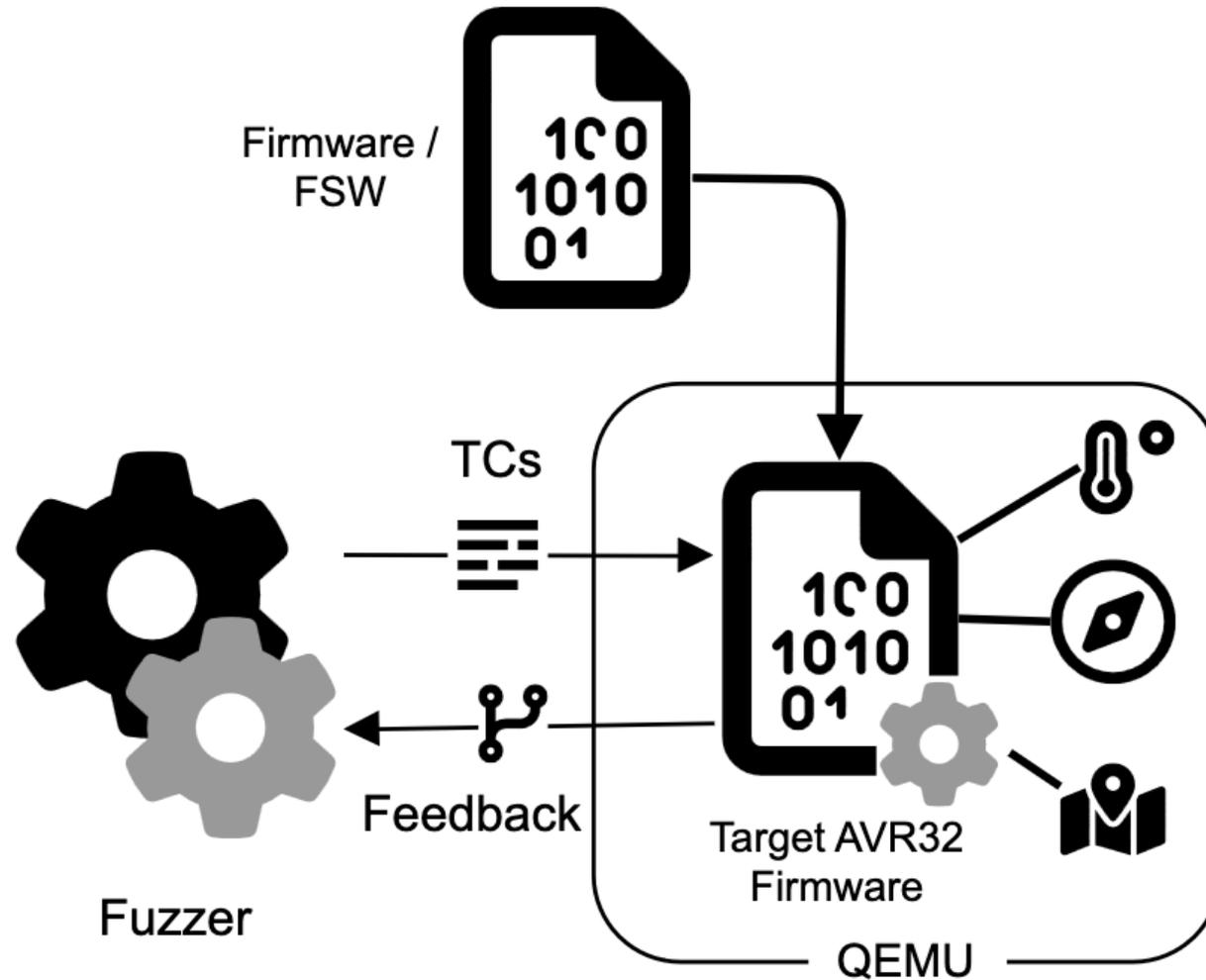


Subsystem Extraction

Issues:

- Many global objects
 - Require manual initialitation and code extraction
- Linux incompatible low-level code
- Extensive manual changes required
- No interactions between components

Persistent Mode Fuzzing

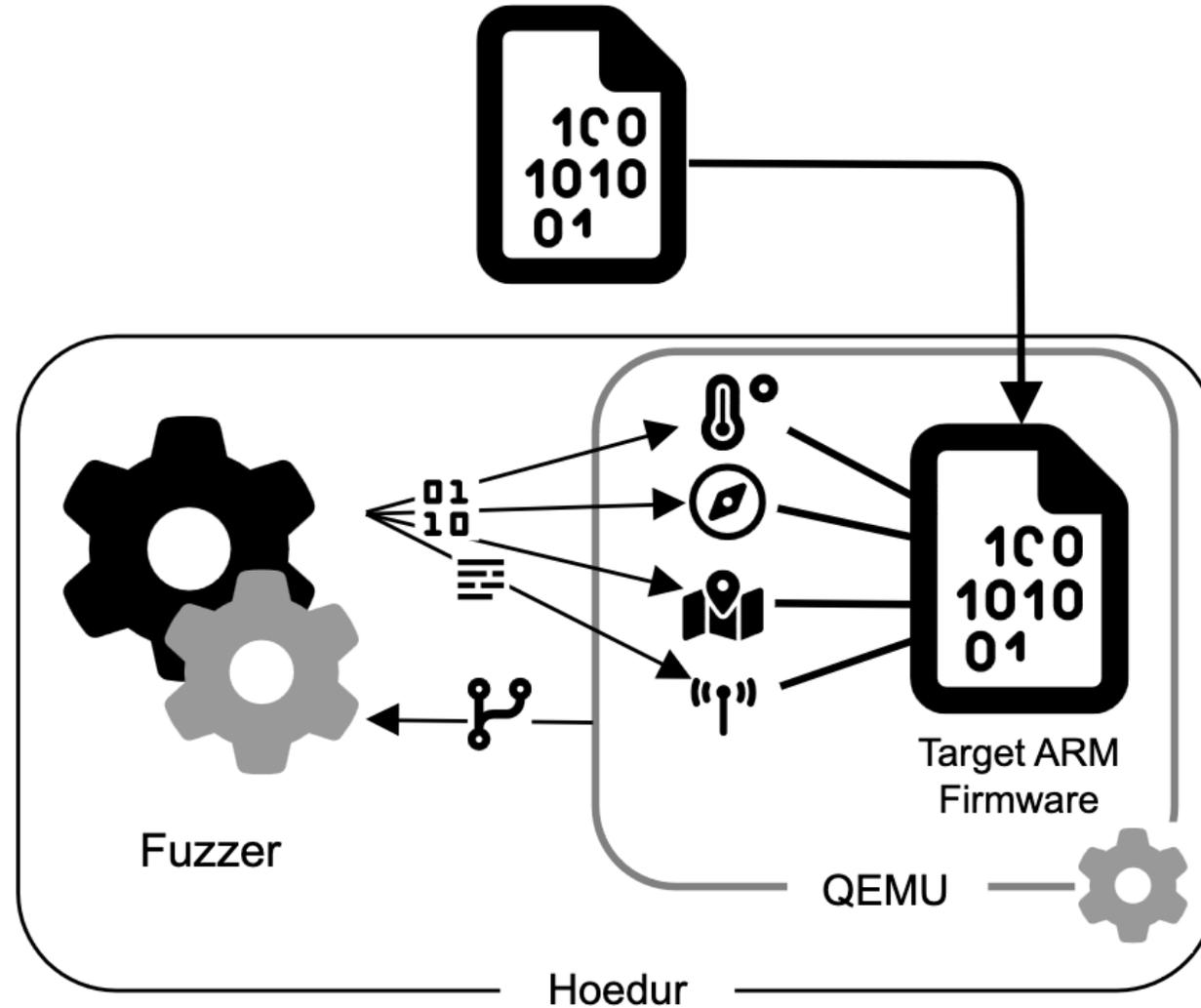


Persistent Mode Fuzzing

Observations

- Skipped bootprocess due to persistent mode
- Potentially non-reproducible bugs due to persistent mode
- Missing peripherals
 - Peripherals with static responses

Firmware Rehosting



Firmware Rehosting

Observations

- Peripheral modelling replaces specific peripheral simulation
- Snapshotting replaces persistent mode
 - But does not have accumulated state
- Read-only regions allow to detect "Dangerous TCs"

Results

Usual Metric: Code Coverage

Results

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Results

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Here: TC Coverage

Results

~~Usual Metric: Code Coverage~~

Here: TC Coverage

Metric	Subsys. Extraction	Persistent Mode Fuzzing	Firmware Rehosting
TC Handlers Reached	-	59/59 (100%)	128/128 (100%)
Code Coverage in TC Handlers	-	1300/1704 (76%)	763/981 (78%)

Results

~~Usual Metric: Code Coverage~~

Here: TC Coverage

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Roadblocks

- Hashes & CRC-Sums
- Large Value Comparisons
- Grammer Formats
- ...

Q&A



- Fuzzing introduction
- Five satellite fuzzing challenges
- Three fuzzing setups with no hardware
- Evaluation



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